Description

Fabrication method for a semiconductor structure having a partly filled trench

The present invention relates to a fabrication method for a semiconductor structure having a partly filled trench.

Although applicable in principle to any desired integrated circuits, the present invention and the problem area on which it is based are explained with regard to semiconductor structures in silicon technology.

Figures 2a-d show diagrammatic illustrations of successive method stages of a fabrication method for a semiconductor structure having a partly filled trench in order to illustrate the problem area on which the invention is based.

In Figure 2a, reference symbol 1 designates a silicon semiconductor substrate into which a trench 2 has been etched by means of a hard mask 5. Said trench 2 has been filled with a filling 10 in such a way that the filling 10 projects above a surface OF of the hard mask 5 by a first height h1, the filling 10 projecting both in the region of the trench 2 and in the region of the periphery 20 of the trench 2. Such a filling 10 can be provided by means of a customary CVD deposition process, by way of example.

The following steps are then carried out for the planarization and sinking of the filling 10 in the trench 2, that is to say for the provision of a partly filled trench 2.

As illustrated in Figure 2b, firstly a first plasma etching step is carried out using an etchant

composition comprising $SF_6/Ar/Cl_2$, a high plasma power being applied, which has the effect that this first etching step proceeds at a relatively high etching rate. The reaching of the surface OF of the hard mask 5 is detected by an optical end point identification, although the latter has a certain delay, so that, in the event of the actual end point identification, the filling 10 has already sunk by a depth T0 in the trench 2. In particular, said depth T0 has a specific fluctuation range $\Delta 1$.

With the triggering of the end point identification, the etchant composition in the plasma reactor is changed over from $SF_6/Ar/Cl_2$ to SF_6/Ar without interrupting the etching process. The reason for this is that an etchant composition of SF_6/Ar is not expedient in the preceding planarization step since such an etchant composition would have poor uniformity on the large surface OF.

The plasma power is also changed over at the same time as the etchant composition is changed. This has the effect that, during a specific stabilization time period of typically a few seconds, the etching rate and uniformity of the etching process change in a more or less poorly definable manner.

Accordingly, the filling 10 has sunk by a depth T1 with a fluctuation range $\Delta 2$ in the trench 2 before the beginning of the actual sinking step with the stabilized etchant composition.

This in turn has the effect that the start depth T1 for the subsequent sinking step can be determined very imprecisely. Since the sinking step is carried out with a fixedly prescribed time, this means that the final desired sinking depth T likewise varies with a not inconsiderable fluctuation range $\Delta 3$.

The problem area on which the present invention is based consists in providing an improved fabrication method for a semiconductor structure having a partly filled trench which makes it possible to obtain smaller fluctuations in the final sinking depth.

According to the invention, this problem is solved by means of the fabrication method specified in claim 1.

The particular advantages of the fabrication method according to the invention are that the method according to the invention enables the final sinking depth to be established with a very small fluctuation range.

The idea on which the present invention is based consists in the fact that essentially the same gas composition and plasma power are used for the planarization and the subsequent sinking and the stabilization step can be obviated as a result.

Advantageous developments and improvements of the subject matter of the invention are found in the subclaims.

In accordance with one preferred development, a planarization of the filling is carried out in a zeroth etching step before the first etching step in such a way that the filling projects above the surface of the semiconductor structure by a second height, the filling covering the trench and the periphery of the trench, the zeroth etching step having a higher etching rate than the first etching step. This has the advantage that firstly a relatively fast planarization is carried out, the latter being slowed down, however, before the touch-down. This means that the touch-down instant and thus the beginning of the sinking can be detected very reliably and, moreover, the overall process can be accelerated.

In accordance with a further preferred development, essentially the same etchant composition as for the first and second etching steps but an increased plasma power are used for the zeroth etching step.

In accordance with a further preferred development, at least the first etching step is carried out with a first time duration which is determined by an end point identification.

In accordance with a further preferred development, the zeroth etching step and the second etching step are carried out with a predetermined zeroth and second time duration. However, in principle, an end point identification could be employed for these etching steps as well.

In accordance with a further preferred development, the second etching step is carried out with a second time duration which is determined by an end point identification. On account of the defined start depth for the sinking step, the error in the end point determination is also reduced in this step.

In accordance with a further preferred development, the etchant composition contains SF_6, Ar and Cl_2.

In accordance with a further preferred development, the semiconductor structure comprises a semiconductor substrate and a mask situated thereon, the mask being used for the etching of the trench.

In accordance with a further preferred development, the end point identification is carried out by interferometry.

Exemplary embodiments of the invention are illustrated in the drawings and explained in more detail in the description below.

Figures 1a-d show diagrammatic illustrations of successive method stages of a fabrication method for a semiconductor structure having a partly filled trench as an embodiment of the present invention; and

Figures 2a-d show diagrammatic illustrations of successive method stages of a fabrication method for a semiconductor structure having a partly filled trench in order to illustrate the problem area on which the invention is based.

In Figures 1 and 2, identical reference symbols designate identical or functionally identical constituent parts.

The starting situation in accordance with Figure 1a is the same as that which has already been explained with reference to Figure 2a.

As illustrated in Figure 1b, a zeroth plasma etching step is then effected for the purpose of planarization using an etchant composition of $SF_6/Ar/Cl_2$ with a high power and a predetermined time, which step brings about planarization of the filling 10 in such a way that the filling 10 projects above the surface OF of the hard mask 5 by a second height h2. In this case, the filling 10 still covers the trench 2 and the periphery 20 of the trench 2.

After this predetermined time in this example, the etchant composition is not altered or is only altered to an insignificant extent, but the plasma power is

significantly reduced, which entails a reduction of the etching rate. Afterward, etching is effected at a reduced etching rate until the filling 10 is essentially planar with the surface OF of the hard mask 5. In this case, on account of the reduced etching rate, the end point can be determined relatively precisely by means of an optical end point identification.

Proceeding from the identified end point, a sinking etching step is carried out with a predetermined time duration and an etchant composition that has not been altered or has been altered to an insignificant extent, in order finally to attain the desired sinking depth T, as is illustrated in Figure 1d.

In accordance with what was stated above, in this embodiment of the method according to the invention, the final sinking depth T has a significantly smaller fluctuation range than the fluctuation range $\Delta 3$ already explained with reference to Figure 2d.

Although the present invention has been described above on the basis of a preferred exemplary embodiment, it is not restricted thereto, but rather can be modified in diverse ways.

In particular, the selection of the mask and substrate materials [lacuna] the arrangement thereof are only by way of example and can be varied in many different ways.

Although an end point identification was used only for the first etching step in the above example, it can, of course, also be used for the further etching steps.

One example of an insignificant change to the etchant composition in the above example would be a slight

shift in the Cl/SF_6 ratio whilst keeping the total flow constant in the range of up to 10%.